REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application. The patentablity of the claims is discussed below.

I. The Claimed Invention

The present invention, as recited independent Claim 1, for example, is directed to a microprocessor comprising a processing unit, and a memory connected to the processing unit and comprising an addressable memory space for a lower memory area and an extended memory area. The microprocessor includes an address bus connecting the processing unit to the memory, and comprising a lower address bus for accessing the lower memory area, and an extended address bus for accessing the extended memory area, and means for executing instructions of an instruction set executable by the processing unit. The instruction set comprises instructions for accessing a first instruction group comprising instructions for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area. The microprocessor also comprises means for forcing to zero an extended address transmitted by the extended address bus when executing an instruction in the first instruction group so that the lower memory area is accessed.

Independent Claim 11 includes a circuit for forcing to zero an extended address and a set of instructions executable by the processing unit. The instructions include a

first instruction group for accessing the lower memory area, and a second instruction group distinct from the first instruction group and only comprising all the instructions for accessing the extended memory area. Independent Claim 21 is a corresponding method claim of independent Claim 1.

II. The Claims Are Patentable

The Examiner rejected independent Claims 1, 11, and 21 as being disclosed by Ronen et al. Ronen et al. discloses an apparatus and methods for porting a 32-bit application to 32-bit address space in a 64-bit processing environment. The apparatus includes a processing unit, a memory, and a 64-bit address register. An instruction core receives instructions from the memory and, when executed, generates an address reference that includes 64 bits and is stored in the 64-bit register. When the address space control flag is set, the instruction core can truncate the 64 bit generated address to 32 bits. If the ported 32-bit application uses a signed address space, the generated address reference can be extended up to 64 bits. If the address space is unsigned address space, the truncated generated references can be zero extended to 64 bits. Additionally, a format control flag can specify whether an address is sign extended or zero extended.

Applicants respectfully submit that the Examiner has mischaracterized Ronen et al. in that Ronen et al. fails to disclose lower and extended address busses and instructions for accessing a first instruction group comprising instructions for accessing the lower memory area.

Additionally, Ronen et al. also fails to disclose a second instruction group distinct from the first instruction group and only comprising all of the instructions for accessing the extended memory area. Instead, Ronen et al. discloses all instructions as being executable by the instruction core and being able to access both the lower memory area and the extended memory area depending on the value of the address control flag. (See Col. 3, lines 11-18). The address control flag instructs the instruction core to truncate the 64-bit generated address to 32 bits. (See Col. 3, lines 11-18). Accordingly, Ronen et al. fails to disclose an instruction set executable by a microprocessor comprising instructions for accessing a first and second distinct instruction groups, only the second group comprising all the instructions for accessing the extended memory area.

Still further, Ronen et al. fails to disclose a means for forcing to zero, an extended address transmitted by the extended address bus when executing an instruction in the first instruction group so that the lower memory areas is accessed. Instead, Ronen et al. discloses zero-extending a 32-bit truncated address to 64 bits based on a setting of the address control flag. In other words, a 64-bit instruction, an instruction that accesses both the lower and upper memory areas, can be truncated to 32 bits based on a flag setting so that the upper bits are set to zero. Thus, an instruction that originally accessed both the upper and lower memory areas becomes limited to the lower memory area. In contrast, in the independent claims of the present invention, an instruction

meant only to access the lower memory area, and yet that attempts to access the upper memory area, the memory location will be forced to zero so as to cnly allow access to the lower memory area.

Accordingly, it is submitted that independent Claims 1, 11 and 21 are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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